CLAIMS

1. An interface system comprising:
a transmitting subsystem; and
a receiving subsystem, including:
a plurality of recovery circuits, with each one of the plurality of recovery circuits dedicated to recover N parallel data streams from a single serial bit stream; and
an aligner receiving multiple ones of the N parallel data streams, determining the degree of misalignment among groups of multiple ones of the N parallel data streams and repositioning to compensate for said misalignment.

2. The interface system of claim 1 wherein N=4.

3. The interface system of claim 1 further including a first module operatively coupled to the transmitting subsystem.

4. The interface system of claim 3 further including a second module operatively coupled to the receiving subsystem.

5. The interface system of claim 1 wherein the aligner includes
parallel sets of storage devices;
a plurality of multiplexers wherein each multiplexer is operatively coupled to a selected set of the parallel sets of storage devices; and
a controller that generates control signals that drive each of the multiplexer.

6. The interface system of claim 4 further including a memory sub-system operatively coupled to the plurality of multiplexers.

7. The interface system of claim 5 wherein each one of the parallel sets of storage devices includes M serially coupled multi-bit latches.

8. The interface system of claim 7 wherein M=3.

9. An aligner including:

parallel sets of storage devices;

a plurality of multiplexers wherein each multiplexer is operatively coupled to a selected set of the parallel sets of storage devices; and

a controller that generates control signals that drive each of the multiplexer.

10. The aligner of claim 9 wherein the controller includes a processor executing a program.

11. A method of processing data comprising the steps of:

receiving multiple streams of serial data;

generating from each one of the multiple stream of serial data a group of parallel bit streams;

storing in a computer memory information representing different groups of parallel bit streams;

searching the memory with a programmed computer to detect a predetermined bit pattern in said information; and

using said programmed computer to adjust the predetermined bit pattern for all groups until said bit pattern is linearly aligned within said computer memory.

12. The method of claim 11 wherein the predetermined bit pattern includes 0101.